DATA SHEET

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- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4059B
LSI
Programmable divide-by-N counter

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

PROGRAMMABLE DIVIDE-BY-N COUNTER

The HEF4059B is a divide-by-n counter which can be programmed to divide an input frequency by any number *n* from 3 to 15 999. The output signal is a one clock-cycle wide pulse and occurs at a rate equal to the input frequency divided by *n*. The single output (O) has TTL drive capability. The down counter is preset by means of 16 jam inputs (J1 to J16); continued on next page.

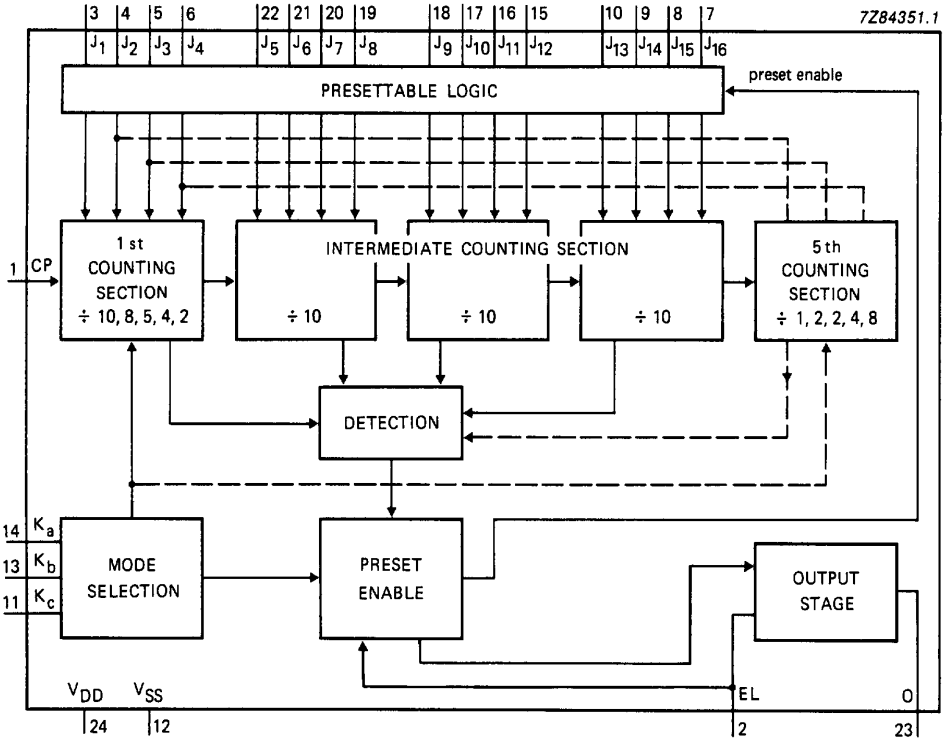

Fig. 1 Functional block diagram.

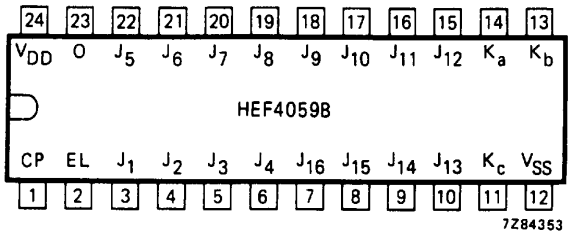

Fig. 2 Pinning diagram.

PINNING

CP	clock input
K_a, K_b, K_c	mode select inputs
J_1 to J_{16}	programmable jam inputs (BCD)
EL	latch enable input
O	divide-by-n output

HEF4059BP(N): 24-lead DIL; plastic (SOT101-1)
HEF4059BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
HEF4059BT(D): 24-lead SO; plastic (SOT137-1)
( ): Package Designator North America

FAMILY DATA | see Family Specifications

I_{DD} LIMITS catagory LSI

The three mode selection inputs K_a, K_b and K_c determine the modulus ('divide-by' number) of the first and last counting sections in accordance with Table 1.
Every time the first (fastest) counting section goes through one cycle, it reduces, by 1, the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section (which consists of flip-flops that are not needed for operating the first counting section).
For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands.
This counting mode is selected when K_a, K_b and K_c are set to HIGH. In this case input J_1 is used to preset the first counting section and J_2 to J_4 are used to preset the last (5th) counting section.
If ÷ 10 mode is desired for the first section, K_a is set HIGH, K_b to HIGH and K_c to LOW. The jam inputs J_1 to J_4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters, presettable by means of the jam inputs J_5 to J_{16}.
When clock pulses are applied to the clock input after a number *n* has been preset into the counter, the counter counts down until the DETECTION circuit detects the zero state. At this time the PRESET ENABLE circuit is enabled to preset again the number *n* into the counter and to produce an output pulse.
The preset of the counter to a desired ÷ *n* is achieved as follows:

n = (MODE*) (1000 x decade 5 preset + 100 x decade 4 preset + 10 x decade 3 preset + 1 x decade 2 preset) + decade 1 preset.
* MODE = first counting section divider (10, 8, 5, 4 or 2).

To calculate preset values for any *n* count, divide the *n* count by the selected mode. The resultant is the corresponding preset values of the 5th to the 2nd decade with the remainder being equal to the 1st decade value.

$$\text{preset value} = \frac{n}{\text{mode}}.$$

If *n* = 8479, and the selected mode = 5, the preset value = 8479 ÷ 5 = 1695 with a remainder of 4, thus the jam inputs must be set as follows:

4			1	5				9				6			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L

The mode select inputs permit frequency-synthesizer channel separations of 10, 12,5, 20, 25 and 50 parts. These inputs set the maximum value of *n* at 9999 (when the first counting section divides by 5 or 10) or at 15 999 (when the first counting section divides by 8, 4 or 2).
The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 count pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the ÷ 8 mode, the number from which the intermediate counting section begins to count-down can be preset to:

3rd decade: 1500
2nd decade: 150
1st decade: 15
1665

The last counting section can be preset to a maximum of 1, with a place value of 1000. The total of these numbers (2665) times 8 equals 21 320. The first counting section can be preset to a maximum of 7. Therefore, 21 327 is the maximum possible count in the ÷ 8 mode. The highest count of the various modes is shown in Table 1, in the column entitled 'extended counter range'. Control inputs K_b and K_c can be used to initiate and lock the counter in the 'master preset' mode. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that mode as long as K_b and K_c both remain LOW. The counter begins to run down from the preset state when a counting mode other than the 'master preset' mode is selected. Whenever the 'master preset' mode is used, control signals K_b = L and K_c = L must be applied for at least 3 full clock pulses. After the master preset mode inputs have been changed to one of the counting modes, the next positive-going clock transitition changes an internal flip-flop so that the count-down can begin at the second positive-going clock transition. Thus, after a 'master preset' mode, there is always one extra count before the output goes HIGH. Figure 3 illustrates the operation of the counter in mode ÷ 8 starting from the preset state 3.

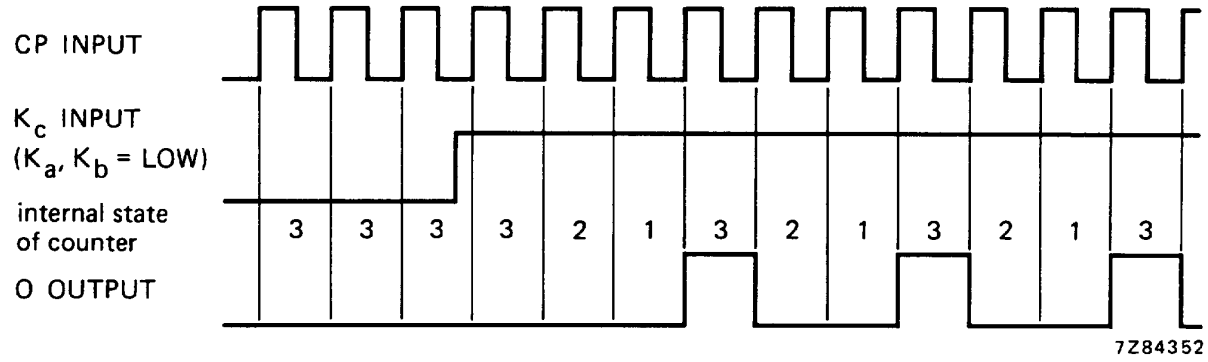

Fig. 3 Total count of 3.

If the 'master preset' mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the 'master preset' mode is not used the counter is preset in accordance with the 'jam inputs when the output pulse appears. A HIGH level at the latch enable input (EL) will cause the counter output to go HIGH once an output pulse occurs, and remain in the HIGH state until EL input returns to LOW. If the EL input is LOW, the output pulse will remain HIGH for only one cycle of the clock input signal.

When K_a = L, K_b = H, K_c = L and EL = L, the counter operates in the 'preset inhibit' mode, with which the dividend of the counter is fixed to 10 000, independent of the state of the jam inputs.

When in the same state of mode select inputs EL = H, the counter operates in the normal ÷ 10 mode, however, without the latch operation at the output.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

FUNCTION TABLE

latch enable input	mode select inputs			first counting section decade 1			last counting section decade 5			counter range		operation
LE	K_a	K_b	K_c	mode	max. preset state	jam inputs used	divide by	max. preset state	jam inputs used	BCD max.	binary max.	
H	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331	timer mode
H	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663	
H	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329	
H	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327	
H	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
L	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331	divide-by-n mode
L	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663	
L	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329	
L	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327	
L	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
H	L	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
L	L	H	L	preset inhibited			preset inhibited			fixed 10 000	–	divide-by-10 000 mode
X	X	L	L	master preset			master preset			–	–	master preset mode

Where:

H = HIGH voltage level
L = LOW voltage level
X = don't care

Note

It is recommended that the device is in the master preset mode (K_b = K_c = logic 0) in order to correctly initialize the device prior to start up.

DC CHARACTERISTICS V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C)			unit	
			–40 min.	+25 min.	+85 min.		
Output (sink) current LOW	4,75	I_{OL}	2,7	2,3	1,8	mA	V_O = 0,4 V; V_I = 0 or 4,75 V
	10		9,5	8	6,3	mA	V_O = 0,5 V; V_I = 0 or 10 V
	15		24	20	16	mA	V_O = 1,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	0,8	0,7	0,5	mA	V_O = 4,6 V; V_I = 0 or 5 V
	10		2,4	2	1,6	mA	V_O = 9,5 V; V_I = 0 or 10 V
	15		8,4	7	5,6	mA	V_O = 13,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	2,4	2	1,6	mA	V_O = 2,5 V; V_I = 0 or 5 V

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	
Dynamic power dissipation per package (P); n = 3	5	1 100 f_i + Σ($f_o C_L$) x V_{DD}^2	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5 500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	15 000 f_i + Σ($f_o C_L$) x V_{DD}^2	
n = 1000	5	500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	10	3 500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	9 000 f_i + Σ($f_o C_L$) x V_{DD}^2	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays	5			90	180	ns	78 ns + (0,25 ns/pF) C_L
CP → O	10	t_{PHL}		45	90	ns	40 ns + (0,10 ns/pF) C_L
HIGH to LOW	15			35	70	ns	32 ns + (0,07 ns/pF) C_L
	5			100	200	ns	76 ns + (0,48 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	40 ns + (0,20 ns/pF) C_L
	15			40	80	ns	33 ns + (0,15 ns/pF) C_L
Output transition times	5			30	60	ns	10 ns + (0,40 ns/pF) C_L
HIGH to LOW	10	t_{THL}		15	30	ns	6 ns + (0,18 ns/pF) C_L
	15			10	20	ns	4 ns + (0,13 ns/pF) C_L
	5			45	90	ns	10 ns + (0,70 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		25	50	ns	9 ns + (0,33 ns/pF) C_L
	15			16	32	ns	5 ns + (0,23 ns/pF) C_L
Maximum clock pulse frequency	5		3,5	7		MHz	
	10	f_{max}	7,5	15		MHz	
	15		10,0	20		MHz	